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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,172	01/22/2000	Deborah T. Marr	2207/7942	6827
7590	04/28/2005		EXAMINER	
Kenyon & Keynon 333 W. San Carlos Street Suite 600 San Jose, CA 95110			CHEN, TE Y	
			ART UNIT	PAPER NUMBER
			2161	

DATE MAILED: 04/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/490,172	MARR, DEBORAH T.	
<b>Examiner</b>		<b>Art Unit</b>	
Susan Y. Chen		2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 15 July 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,3-11 and 13-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,3-11 and 13-21 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

***Response to Amendment***

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/15/2004 has been entered.

This office action is in response to amendment filed on 07/15/2004.

Claims 1, 3-11 and 13-21 are pending for examination. Claims 1, 10 and 20 have been amended; claim 21 is newly added.

***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 3-11 and 13-21 are rejected under the judicially created doctrine of double patenting over claims 1-17 of U. S. Patent No. 6,658,447. Although the conflicting claims are not identical, they are not patentably distinct from each other. Because claims 1, 3-11 and 13-21 of instant application merely repeat features of claims 1-17 in the '447 patent, except that the instant application cited a broader scope for establishing multi-thread priority in a processor.

Since the difference of the claimed subject matters in scope is de minimis and unrelated to the overall aesthetic appearance of the claims being compared; and it would have been obvious for one of ordinary skill in the art, at the time the invention was made to remove intended limitations from the claims for the purpose to extend a more broader coverage of his/hers invention.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-10 and 20-21, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 1, 10 and 20, it is not understood how the claimed "value is being selected [i.e., Which unit performs the selection? What is the purpose to do the selection?]

As to claims 3-9 and 21, these claims have the same defects as their base claims hence are rejected for the same reason.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-11 and 13-21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (U.S. Patent. No. 6,105,127), in view of Huwitt et al. (U.S. Patent No. 6,339,808) and further in view of Borkenhagen et al. (U.S. Patent No. 6,567,839).

Kimura et al's patent (EP 0827071) was provided twice by applicant via IDS filed on 10/03/2001 and 08/07/2002.

As to claim 20, Kimura et al. (hereinafter referred as Kimura) disclosed an apparatus for establish thread priority in a processor [Title; Abstract; Fig. 2] comprising:

- a) a memory including Task priority Register (TPR) to store a value to indicate which one of the threads has a higher priority [e.g., Fig (s). 6-7; Fig. 15; col. 8, lines 59 – col. 9, line 8, etc.];
- b) a resource allocated between the plurality of threads depending on a priority assigned to each thread in the memory [e.g., Abstract, lines 10-15; the shared resource functional unit, col. 6, lines 19-30; col. 8, lines 17-27].

Kimura does not expressly disclose an Advanced Programmable Interrupt Controller (APIC) with a counter loaded with a predetermined value.

However, Hewitt et al. (hereinafter referred as Hewitt) discloses Advanced Programmable Interrupt Controller (APIC) [e.g., 221, 223, 225, 227, Fig. 2] with a counter [e.g., the FEE0 0390H Current Count Register for Timer of Table 1, col. 5, line 3 at seq.] loaded with a predetermined value of Programmable Interrupt Controller (PIC) [e.g., the Task Priority Register, Arbitration Priority Register, Processor Priority Register of Table 1 at col. 5; col. 4, lines 22-26; col. 8, line 38 - col. 9, line 10; Fig. (s), 2-6]. Thus, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kimura and Hewitt to further modify the combined system with a counter loaded with a predetermined value of Programmable Interrupt Controller (PIC), because by doing so, the combined system would reduce the latency inherent in a complex serial bus architecture [e.g. Hewitt: col. 3, lines 7-27].

The combined system of Kimura and Hewitt fails to expressly disclose that the predetermined value of the counter is for plurality of threads depending on the priority assigned to each thread.

However, Borkenhagen et al. (hereinafter referred as Borkenhagen) discloses a thread switch control technique having a counter with the predetermined value for plurality of threads depending on the priority assigned to each thread [col. 5, lines 32 – col. 6, line 11]. Thus, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kimura, Hewitt and Borkenhagen to further modify the Programmable Interrupt Controller (PIC) of the combined system with a counter loaded with a predetermined value as taught by Borkenhagen, such that the combined system will provided a counter with the predetermined value for plurality of threads depending on the priority assigned to each thread. Because by doing so, the system will not only having the advantage to reduce the latency inherent in a complex serial bus architecture but also including the feature of altering the priority which allows changing the frequency of thread switching, increasing execution cycles for a critical task, and decreasing the number of processing cycles lost by the high priority thread because of thread switch latency [Borkenhagen: col. 6, lines 5-11].

As to claim 11, this claim merely recited the same features as claim 20 with less limitations, hence are rejected for the same reason.

As to claims 13-19 and 21, in addition to the features of claims 11 and 20, Kimura, Hewitt and Borkenhagen further disclosed that access to the resource is given to the thread with higher priority and the usage of the resource [e.g., Kimura: col. 4, line 64-col. 5, line 10; col. 6, lines 26-30], wherein the resource is a decode unit [Kimura: 1-3, Fig. 2; instruction decode units 1-3; Fig. 13; 111-113, Fig. 15] in a processor system, the decode unit correspond to a bus unit [for example, Kimura: Internal Bus and Instruction Decode Units 1-3, Fig. 13] which including queues [for example, Kimura: 30, 40, 50, Fig. 2; 140, Fig. 15] to storing bus requests from a plurality of threads [Kimura: Fig. 2; Fig. 8; Fig. 11; Fig. 13] and control logic [Kimura: 60, Fig. 2; 60, 150, 170, Fig. 15] couple to the queues to select based on the priority value [Kimura: Fig. 2; Fig (s). 8-9; Fig. 11; Fig. 13; Fig. 15].

As to claims 1, 3-10, the steps in the claimed method is deemed to be made obvious by the functions of the apparatus structure of claims 11 and 13-20 in the combination discussed above, hence were rejected for the same reasons.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-20 are based on amended subject matter that have been considered but are moot in view of the new ground(s) of rejection (i.e., 35 U.S.C. 112 second paragraph rejection).

### ***Conclusion***

To expedite the process of re-examination, the examiner requests that all future correspondences in regard to overcoming prior art rejections or other issues (e.g. 35 U.S.C. 112) set forth by the Examiner prior to the office action, that applicant should provide and link to the most specific page and line numbers of the disclosure where best support is found (see 35 U.S.C. 132).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Gravenstein et al. (U.S. Patent No. 5,799,182) which discloses a system to process computer instructions via multi-thread and program counter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Susan Y. Chen whose telephone number is 571-272-4016. The examiner can normally be reached on Monday - Friday from 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 571-272-4023. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Susan Y Chen  
Examiner  
Art Unit 2161

April 20, 2005

  
UYEN LE  
PRIMARY EXAMINER